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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	10/628,614	
	Filing Date	July 28, 2003	
	First Named Inventor	Roger Y. B. Young, et al.	
	Art Unit	2878	
	Examiner Name	Le, Que Tan	
Total Number of Pages in This Submission	32	Attorney Docket Number	03-0460

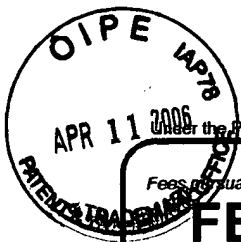
ENCLOSURES (Check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input checked="" type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input type="checkbox"/> Other Enclosure(s) (please identify below):
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	L. Jon Lindsay, Attorney at Law		
Signature			
Printed name	L. Jon Lindsay		
Date	April 6, 2006	Reg. No.	36,855

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Typed or printed name	L. Jon Lindsay	Date	April 6, 2006

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FEE TRANSMITTAL

For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 500

Complete if Known

Application Number	10/628,614
Filing Date	July 28, 2003
First Named Inventor	Roger Y. B. Young, et al.
Examiner Name	Le, Que Tan
Art Unit	2878
Attorney Docket No.	03-0460

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 12-2252 Deposit Account Name: LSI Logic Corporation

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description

Each claim over 20 (including Reissues)

Fee (\$)
50Small Entity Fee (\$)
25

Each independent claim over 3 (including Reissues)

200

100

Multiple dependent claims

360

180

Total Claims Extra Claims Fee (\$)

Fee Paid (\$)

- 20 or HP =

x

=

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims Extra Claims Fee (\$)

Fee Paid (\$)

- 3 or HP =

x

=

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
- 100 =	/ 50 =	(round up to a whole number) x	=	

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Fees Paid (\$)

Other (e.g., late filing surcharge): Filing an Appeal Brief per \$ 41.20(b)(2)

500

SUBMITTED BY

Signature		Registration No. 36,855	Telephone 303-518-1839
Name (Print/Type)	Jon Lindsay	(Attorney/Agent)	Date April 6, 2006

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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AF
11/11

Appl. No. : 10/628,614 Confirmation No. 4439
Applicant : Roger Y. B. Young, et al.
Filed : July 28, 2003
TC/A.U. : 2878
Examiner : Le, Que Tan
Title : Wafer Edge Defect Inspection Using Captured Image
Analysis (as amended)

Docket No. : 03-0460
Customer No. : 024319

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Appeal Brief

Sir:

In response to the Office Action of December 1, 2005, and in consideration of the Notice of Appeal filed February 8, 2006, Applicant submits this Appeal Brief.

04/12/2006 TBESHAH1 00000007 122252 10628614

01 FC:1402 500.00 DA

Real party in interest

The real party in interest is LSI LOGIC CORPORATION, a corporation of Delaware, having a place of business at Milpitas, California.

Related appeals and interferences

There are no appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 2-7 and 10-20 currently stand as rejected. Claims 1, 8 and 9 are canceled. The claims appealed are claims 2-7 and 10-20.

Status of Amendments

There has been no amendment filed subsequent to final rejection.

Summary of claimed subject matter

Embodiments of the invention include a method of inspecting a semiconductor wafer 136 for defects 172-184 using captured image analysis comprising: positioning the wafer 136 with an edge thereof relative to an image capturing device 132, 134 (page 10, line 24 to page 11, line 11); positioning the image capturing device 132, 134 at a desired angle relative to the edge of the wafer 136 (page 12, lines 1-4); rotating the wafer 136 (page 10, lines 19-21); scanning the edge of the rotating wafer 136 with the image capturing device 132, 134 (page 10, lines 19-21); recording an image of a desired portion of the edge of the scanned wafer 136 from the image capturing device 132, 134 into a database 126 (page 8, lines 19-20; page 11, lines 21-23); instructing a computer 128 to analyze the recorded images of the scanned wafer 136 (page 8, lines 27-29); identifying any defects in the analyzed recorded images (page 8, lines 29-30); and upon identifying any defects, recording defect information related to each defect (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2).

Other embodiments of the invention include a method of inspecting a semiconductor wafer 136 for defects 172-184 using captured image analysis comprising: after a first process step (e.g. at 104): positioning the wafer 136 with an edge thereof relative to an image capturing device 132, 134 (page 10, line 24 to page 11, line 11); rotating the wafer 136 (page 10, lines 19-21); scanning the edge of the rotating wafer 136 with the image capturing device 132, 134 (page 10, lines 19-21); recording an image of the scanned wafer 136 from the image capturing device 132, 134 into a database 126 (page 8, lines 19-20; page 11, lines 21-23); instructing a computer 128 to analyze the recorded images of the scanned wafer 136 (page 8, lines 27-29); identifying any defects in the analyzed recorded images (page 8, lines 29-30); and upon identifying any defects, recording defect information related to each defect (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2). after a second process step (e.g. at 106), repeating the aforementioned steps (page 5, line 27 to page 6, line 13); comparing the defect information recorded

after the first process step to the defect information recorded after the second process step (page 5, line 27 to page 6, line 13); and identifying any new defects as added defects due to the second process step (page 6, line 5; page 12, line 26 to page 13, line 10).

Further embodiments of the invention include a method of inspecting a semiconductor wafer 136 for defects using captured image analysis comprising: after a first process step (e.g. at 104): positioning the wafer 136 with an edge thereof relative to an image capturing device 132, 134 (page 10, line 24 to page 11, line 11); rotating the wafer 136 (page 10, lines 19-21); scanning the edge of the rotating wafer 136 with the image capturing device 132, 134 (page 10, lines 19-21); recording an image of the scanned wafer 136 from the image capturing device 132, 134 into a database 126 (page 8, lines 19-20; page 11, lines 21-23); instructing a computer 128 to analyze the recorded images of the scanned wafer 136 (page 8, lines 27-29); identifying any defects in the analyzed recorded images (page 8, lines 29-30); and upon identifying any defects, recording defect information related to each defect (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2). after a second process step (e.g. at 106), repeating the aforementioned steps (page 5, line 27 to page 6, line 13); comparing the defect information recorded after the first process step to the defect information recorded after the second process step (page 5, line 27 to page 6, line 13); determining whether any defects identified after the first process step have been reduced after the second process step (page 6, line 6; page 9, lines 2-3 and 27-29; page 13, lines 11-14); and identifying any such reduced defects as repaired defects (page 6, line 6; page 9, lines 2-3 and 27-29; page 13, lines 11-14).

Still other embodiments of the invention include a method of inspecting an edge of a semiconductor wafer 136 for defects during fabrication of integrated circuit components on the semiconductor wafer 136 within a fabrication system 100 that includes a plurality of fabrication stations 102-114 arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers 136 (page 5, lines 4-10), comprising: providing a plurality of inspection stations 116-

122 within the fabrication system 100 corresponding to selected ones of the fabrication stations 102-114, each inspection station 116-122 being located in a subsequent processing order to a corresponding one of the selected fabrication stations 102-114 (page 5, line 10 to page 6, line 13); processing a wafer 136 in a first fabrication station (e.g. 104) (page 5, lines 11-18); automatically inspecting an edge of the wafer 136 in a first inspection station (e.g. 116) (page 12, line 26 to page 13, line 14); automatically recording a first set of defects in the edge of the wafer 136 (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2); processing the wafer 136 in a second fabrication station (e.g. 106) (page 5, lines 11-18); automatically inspecting the edge of the wafer 136 in a second inspection station (e.g. 118) (page 12, line 26 to page 13, line 14); and automatically recording a second set of defects in the edge of the wafer 136 (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2).

Other embodiments of the invention include a method of inspecting an edge of semiconductor wafers 136 for defects during fabrication of integrated circuit components on the semiconductor wafers 136 within a fabrication system 100 that includes a plurality of fabrication stations 102-114 arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers 136 (page 5, lines 4-10), comprising: providing a plurality of inspection stations 116-122 within the fabrication system 100 corresponding to selected ones of the fabrication stations 102-114, each inspection station 116-122 being located in a subsequent processing order to a corresponding one of the selected fabrication stations 102-114 (page 5, line 10 to page 6, line 13); processing the wafers 136 in the fabrication stations 102-114 (page 5, lines 11-18); inspecting the edge of the wafers 136 in the inspection stations 116-122 (page 12, line 26 to page 13, line 14); upon inspecting each wafer 136, recording an image of the edge of the wafer 136 (page 8, lines 19-20; page 11, lines 21-23); and correlating each recorded image with the wafer 136 from which it was taken and the process step after which it was taken (page 8, lines 20-25).

Still other embodiments of the invention include a wafer edge defect inspection system 116-122 comprising an image capturing device 132, 134, a database 126 and a computer 128 (page 8, lines 4-6). A wafer 136 can be positioned next to the image capturing device 132, 134 (page 10, line 24 to page 11, line 11). The image capturing device 132, 134 is oriented to view at least a portion of an edge of the wafer 136 (page 12, lines 1-4). The image capturing device 132, 134 automatically generates an image of the edge of the wafer 136 (page 10, lines 19-21). The database 126 is connected to the image capturing device 132, 134 to receive the generated image of the edge of the wafer 136 (page 8, lines 4-20). The database 126 automatically stores the received image for subsequent analysis (page 9, lines 5-15). The computer 128 is connected to the database 126 to retrieve the stored image upon instruction from a user to perform image analysis to locate any defects in the edge of the wafer 136 (page 8, line 27 to page 9, line 8).

Grounds of rejection to be reviewed on appeal

Whether claims 4 and 16 are unpatentable under 35 USC 102(e) over *Tsuji* (United States Patent 6,906,794).

Whether claims 3, 5-7, 10-15 and 17-20 are unpatentable under 35 USC 103(a) over *Tsuji*.

Argument

I. Rejections under 35 U.S.C. 102(e) over *Tsuji*:

a. Claim 4:

Applicant respectfully traverses the rejection of **claim 4** under 35 U.S.C. 102(e) as being anticipated by *Tsuji*. **Claim 4** is independent.

Independent **claim 4** recites:

positioning the image capturing device at a desired angle relative to the edge of the wafer.

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. Instead, *Tsuji* does not appear to disclose that the imaging device 100 and the objective lens 60 can be “positioned.” Therefore, it appears that the angle of the imaging device is **fixed**. The final office action states that “*Tsuji* discloses a positioning device (movement stage 30, rotatable table 21, and the alignment mechanism, column 7).” Applicant respectfully submits, however, that this positioning device in *Tsuji* relates to the positioning of the wafer 2, not to the imaging device 100 or objective lens 60 (column 4, lines 24-31). Applicant respectfully submits, therefore, that independent **claim 4** is not anticipated by, is not obvious in view of, and is patentable over *Tsuji* at least because the reference does not teach or fairly suggest **positioning the image capturing device** at a desired angle.

b. Claim 16:

Applicant respectfully traverses the rejection of **claim 16** under 35 U.S.C. 102(e) as being anticipated by *Tsuji*. **Claim 16** is independent.

Independent **claim 16** recites:

an image capturing device ..., the image capturing device **automatically** generating an image of the edge of the wafer;
a database ..., the database **automatically** storing the received image for subsequent analysis.

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. Instead, *Tsuji* appears to disclose that the edge inspection is **manual**, rather than **automatic**, since a user must use the joy stick pointing device 50 to control the position and rotation of the table 21 on which the wafer 2 is placed. (See column 4, lines 41-55; and Fig. 2.) Additionally, operator action is required to stop the rotation of the table 21 and capture an image of the desired portion of the wafer edge (column 6, lines 1-9) and to end the observation of the wafer edge portion (column 6, lines 24-26). The final office action states that "Tsuji states that 'An automatic defect classification software is installed in the image processing section' while the image processing section is automatically performed." (See column 6, lines 15-23.) Applicant respectfully submits, however, that this automation refers to the classification of the defect, **not** to the generating or storing of an image, as claimed in **claim 16**. Applicant respectfully submits, therefore, that independent **claim 16** is not anticipated by, is not obvious in view of, and is patentable over *Tsuji* at least because the reference does not teach or fairly suggest **automatic** generating and storing of an image.

II. Rejections under 35 USC 103(a) over *Tsuji*:

Applicant respectfully traverses the rejection of **claims 3, 5-7, 10-15 and 17-20** under 35 USC 103(a) as being unpatentable over *Tsuji*. The independent claims under this rejection are **claims 6, 7, 10 and 13**.

a. Claims 6 and 7:

Independent **claim 6** recites:

comparing the defect information recorded after the first process step to the defect information recorded after the second process step; and
identifying any new defects as **added defects** due to the second process step.

Independent **claim 7** recites:

comparing the defect information recorded after the first process step to the defect information recorded after the second process step ;
determining whether any defects identified after the first process step have been **reduced** after the second process step; and
identifying any such reduced defects as **repaired defects**.

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. The final office action states (page 4, lines 10-12) that “repeatedly inspecting the same area or portion of an inspected object or wafer for ensuring a complete inspection performance would have been obvious to one of ordinary skill in the inspection art.” Applicant respectfully submits, however, that whereas an “inspection” may imply a review of the results of the inspection and whereas a “repeated inspection” may imply a review of the new results, there is **no** necessary implication or suggestion that the two results will be **compared** to each other. **Additionally**, such repeated inspection and review of results cannot imply or suggest that any “**added defects**” or “**repaired defects**” will specifically be **identified** during the subsequent review of results. Applicant respectfully submits, therefore, that independent **claims 6 and 7** are not anticipated by, are not obvious in view of, and are patentable over *Tsuji* at least because the reference does not teach or fairly suggest **comparing** defect information and/or **identifying** any new defects as **added defects** or reduced defects as **repaired defects**.

b. Claim 10:

Independent **claim 10** recites:

automatically inspecting an edge of the wafer in a first inspection station;
automatically recording a first set of defects in the edge of the wafer;
...
automatically inspecting the edge of the wafer in a second inspection station; and

automatically recording a second set of defects in the edge of the wafer.

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. Instead, *Tsuji* appears to disclose that the edge inspection is **manual**, rather than **automatic**, since a user must use the joy stick pointing device 50 to control the position and rotation of the table 21 on which the wafer 2 is placed. (See column 4, lines 41-55; and Fig. 2.) Additionally, operator action is required to stop the rotation of the table 21 and capture an image of the desired portion of the wafer edge (column 6, lines 1-9) and to end the observation of the wafer edge portion (column 6, lines 24-26). The final office action states that "Tsuji states that 'An automatic defect classification software is installed in the image processing section' while the image processing section is automatically performed." (See column 6, lines 15-23.)

Applicant respectfully submits, however, that this automation refers to the classification of the defect, **not** to the inspecting of the edge or the recording of defects, as claimed in **claim 10**. Applicant respectfully submits, therefore, that independent **claim 10** is not anticipated by, is not obvious in view of, and is patentable over *Tsuji* at least because the reference does not teach or fairly suggest **automatic** inspection and recording of sets of defects.

c. Claim 13:

Independent **claim 13** recites:

correlating each recorded image with the wafer from which it was taken and **the process step after which it was taken**.

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. Instead, *Tsuji* appears to disclose only that image data, related defect data, "the coordinates and the rotating angle of a portion [of the wafer] being observed," and a wafer identification number may be correlated. (See column 6, lines 62-65; column 7, lines 1-6 and 54-56; column 11, lines 34-42.) *Tsuji* does not appear to disclose, however, that this information is correlated with the **process step** after which the

recorded image was taken. The final office action lists several types of information that *Tsuji* may disclose as being stored (page 6, lines 13-16), but none of this information is related to the **process step** after which a recorded image is taken, as claimed in **claim 13**. Applicant respectfully submits, therefore, that independent **claim 13** is not anticipated by, is not obvious in view of, and is patentable over *Tsuji* at least because the reference does not teach or fairly suggest that each recorded image is correlated with the **process step after which it was taken**.

d. Dependent Claims 3, 5, 11, 12, 14, 15 and 17-20:

Claims 5, 11, 12, 14, 15 and 17-20 depend either directly or indirectly from independent claims 4, 10, 13 or 16. Applicant respectfully submits, therefore, that dependent **claims 5, 11, 12, 14, 15 and 17-20** are also not anticipated by, are not obvious in view of, and are patentable over *Tsuji* at least for the same reasons as are independent claims 4, 10, 13 or 16, as explained above.

i. Dependent Claim 3:

Dependent **claim 3** recites:

setting an angle of the image capturing device relative to the edge of the wafer...

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. Instead, whereas *Tsuji* appears to disclose that some parameters can be set, *Tsuji* does not appear to disclose that the claimed parameters in claim 3 can be set. Additionally, as discussed above, *Tsuji* does not appear to disclose that the imaging device 100 and the objective lens 60 can be "positioned," so it appears that the angle of the imaging device is **fixed** and cannot be set. Additionally, Applicant respectfully notes that the final office action does not discuss this limitation. Applicant respectfully submits, therefore, that dependent **claim 3** is not anticipated by, is not obvious in view of, and is patentable over *Tsuji* at least because the

reference does not teach or fairly suggest **setting an angle of the image capturing device** relative to the edge of the wafer.

ii. **Dependent Claims 11 and 12:**

Dependent **claim 11** recites:

determining a difference between the first and second sets of defects.

Dependent **claim 12** recites:

identifying process-induced edge defects from the determined difference between the first and second sets of defects.

Applicant respectfully submits that *Tsuji* does not teach or suggest this limitation. Instead, similar to the arguments above regarding independent claims 6 and 7, although repeated inspections may imply a review of each new set of results, there is no necessary implication or suggestion that the review of the results will **determine a difference** between the results and/or **identify process-induced edge defects** therefrom. Applicant respectfully submits, therefore, that in addition to the above arguments, dependent **claims 11 and 12** are not anticipated by, are not obvious in view of, and are patentable over *Tsuji* at least because the reference does not teach or fairly suggest **determining a difference** between sets of defects and/or **identifying process-induced edge defects** from the determined difference.

iii. **Dependent Claims 14 and 15:**

Dependent **claim 14** recites:

selecting a recorded image ... **by specifying ... the process step after which it was taken.**

Dependent **claim 15** recites:

selecting two recorded images ... by specifying ... the two process steps after which each selected image was taken;
... and

determining whether any **defects were added** to the edge of the specified wafer ...

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. Instead, since *Tsuji* does not appear to disclose that any information is correlated with the **process step** after which the recorded image was taken (see arguments above regarding claim 13), *Tsuji* also does not appear to disclose that a recorded image can be **selected by specifying** the process step. Additionally, similar to the arguments above regarding independent claims 6 and 7, although repeated inspections may imply a review of each new set of results, there is no necessary implication or suggestion that the review of the results will determine whether any **defects were added**. Applicant respectfully submits, therefore, that in addition to the above arguments, dependent **claims 14 and 15** are not anticipated by, are not obvious in view of, and are patentable over *Tsuji* at least because the reference does not teach or fairly suggest that a recorded image can be **selected by specifying** the process step after which it was taken. Additionally, Applicant respectfully submits that in addition to the above arguments, dependent **claim 15** further is not anticipated by, is not obvious in view of, and is patentable over *Tsuji* at least because the reference does not teach or fairly suggest determining whether any **defects were added** to the edge of the specified wafer.

iv. Dependent Claims 18 and 19:

Dependent **claim 18** recites:

the computer compares and analyzes the first and second images together ... to determine **whether any defects have been added** to the edge of the wafer between times that the first and second images thereof are generated.

Dependent **claim 19** recites:

the computer compares and analyzes the first and second images together ... to determine **whether any defects have been repaired** on the edge of the wafer between times that the first and second images thereof are generated.

Applicant respectfully submits that *Tsuji* does not teach or suggest these limitations. Similar to the arguments above regarding independent claims 6 and 7, although repeated inspections may imply a review of each new set of results, there is no necessary implication or suggestion that the review of the results will determine whether any **defects were added or repaired**. Applicant respectfully submits, therefore, that in addition to the above arguments, dependent **claims 18 and 19** are not anticipated by, are not obvious in view of, and are patentable over *Tsuji* at least because the reference does not teach or fairly suggest that it can be determined whether any **defects were added to or repaired on** the edge of the wafer between times that first and second images thereof are generated.

Claims Appendix

Claim 1 (Canceled)

Claim 2: A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

positioning the wafer with an edge thereof relative to a scanning electron microscope;

rotating the wafer;

scanning the edge of the rotating wafer with the scanning electron microscope;

recording an image of the scanned wafer from the scanning electron microscope into a database;

instructing a computer to analyze the recorded images of the scanned wafer;

identifying any defects in the analyzed recorded images; and

upon identifying any defects, recording defect information related to each defect.

Claim 3: A method as defined in claim 2 further comprising:

before scanning the edge of the wafer, setting an angle of the image capturing device relative to the edge of the wafer, a brightness of an illumination source that illuminates the edge of the wafer, and an accelerating voltage of an electron beam.

Claim 4: A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

- positioning the wafer with an edge thereof relative to an image capturing device;

- positioning the image capturing device at a desired angle relative to the edge of the wafer;

- rotating the wafer;

- scanning the edge of the rotating wafer with the image capturing device;

- recording an image of a desired portion of the edge of the scanned wafer from the image capturing device into a database;

- instructing a computer to analyze the recorded images of the scanned wafer;

- identifying any defects in the analyzed recorded images; and

- upon identifying any defects, recording defect information related to each defect.

Claim 5: A method as defined in claim 4 wherein:

- the scanning step further comprises:

- scanning the edge of the wafer from a region interior of a top of the edge to a region exterior of a bottom of the edge.

Claim 6: A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

after a first process step:
positioning the wafer with an edge thereof relative to an image capturing device;
rotating the wafer;
scanning the edge of the rotating wafer with the image capturing device;
recording an image of the scanned wafer from the image capturing device into a database;
instructing a computer to analyze the recorded images of the scanned wafer;
identifying any defects in the analyzed recorded images; and
upon identifying any defects, recording defect information related to each defect.
after a second process step, repeating the aforementioned steps;
comparing the defect information recorded after the first process step to the defect information recorded after the second process step; and
identifying any new defects as added defects due to the second process step.

Claim 7: A method of inspecting a semiconductor wafer for defects using captured image analysis comprising:

after a first process step:
positioning the wafer with an edge thereof relative to an image

capturing device;

rotating the wafer;

scanning the edge of the rotating wafer with the image capturing device;

recording an image of the scanned wafer from the image capturing device into a database;

instructing a computer to analyze the recorded images of the scanned wafer;

identifying any defects in the analyzed recorded images; and
upon identifying any defects, recording defect information related to each defect.

after a second process step, repeating the aforementioned steps;
comparing the defect information recorded after the first process step to the defect information recorded after the second process step;

determining whether any defects identified after the first process step have been reduced after the second process step; and

identifying any such reduced defects as repaired defects.

Claim 8 (Canceled)

Claim 9 (Canceled)

Claim 10: A method of inspecting an edge of a semiconductor wafer for defects during fabrication of integrated circuit components on the semiconductor wafer within a fabrication system that includes a plurality of fabrication stations

arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers, comprising:

providing a plurality of inspection stations within the fabrication system corresponding to selected ones of the fabrication stations, each inspection station being located in a subsequent processing order to a corresponding one of the selected fabrication stations;

processing a wafer in a first fabrication station;

automatically inspecting an edge of the wafer in a first inspection station;

automatically recording a first set of defects in the edge of the wafer;

processing the wafer in a second fabrication station;

automatically inspecting the edge of the wafer in a second inspection station; and

automatically recording a second set of defects in the edge of the wafer.

Claim 11: A method as defined in claim 10 further comprising:

determining a difference between the first and second sets of defects.

Claim 12: A method as defined in claim 11 further comprising:

identifying process-induced edge defects from the determined difference between the first and second sets of defects.

Claim 13: A method of inspecting an edge of semiconductor wafers for defects during fabrication of integrated circuit components on the semiconductor

wafers within a fabrication system that includes a plurality of fabrication stations arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers, comprising:

- providing a plurality of inspection stations within the fabrication system corresponding to selected ones of the fabrication stations, each inspection station being located in a subsequent processing order to a corresponding one of the selected fabrication stations;

- processing the wafers in the fabrication stations;

- inspecting the edge of the wafers in the inspection stations;

- upon inspecting each wafer, recording an image of the edge of the wafer; and

- correlating each recorded image with the wafer from which it was taken and the process step after which it was taken.

Claim 14: A method as defined in claim 13 further comprising:

- selecting a recorded image from among a plurality of the recorded images by specifying the wafer from which it was taken and the process step after which it was taken; and

- determining whether any defects were present on the edge of the specified wafer at a time that the selected recorded image was taken of the edge of the specified wafer by analyzing the selected recorded image.

Claim 15: A method as defined in claim 13 further comprising:

- selecting two recorded images from among a plurality of the recorded

images by specifying the wafer from which both images were taken and the two process steps after which each selected image was taken;

determining any defects that were present on the edge of the specified wafer at times that the two selected recorded images were taken of the edge of the specified wafer by analyzing the two selected recorded images; and

determining whether any defects were added to the edge of the specified wafer between the times that the two selected recorded images were taken by comparing the determined defects from the analyzing of the two selected recorded images.

Claim 16: A wafer edge defect inspection system comprising:

an image capturing device next to which a wafer can be positioned, the image capturing device being oriented to view at least a portion of an edge of the wafer, the image capturing device automatically generating an image of the edge of the wafer;

a database connected to the image capturing device to receive the generated image of the edge of the wafer, the database automatically storing the received image for subsequent analysis; and

a computer connected to the database to retrieve the stored image upon instruction from a user to perform image analysis to locate any defects in the edge of the wafer.

Claim 17: A wafer edge defect inspection system as defined in claim 16, wherein the image capturing device is a first image capturing device, the image

generated thereby is a first image and the wafer edge defect inspection system is incorporated into a fabrication system having a plurality of fabrication stations for processing the wafer and forming integrated circuit components thereon, further comprising:

a second image capturing device next to which the wafer can be positioned, the second image capturing device being oriented to view at least the portion of the edge of the wafer, the second image capturing device automatically generating a second image of the edge of the wafer and being connected to the database to supply the second image to the database;

and wherein:

the database automatically stores the second image for subsequent analysis by the computer;

the first image capturing device is incorporated into the fabrication system to receive the wafer after a first fabrication station performs a first process step on the wafer and the first image capturing device generates the first image of the edge of the wafer after the first process step;

the second image capturing device is incorporated into the fabrication system to receive the wafer after a second fabrication station performs a second process step on the wafer and the second image capturing device generates the second image of the edge of the wafer after the second process step; and

the computer retrieves the stored first and second images upon

instruction from the user to compare and analyze the first and second images together.

Claim 18: A wafer edge defect inspection system as defined in claim 17, wherein:

the computer compares and analyzes the first and second images together upon instruction from the user to determine whether any defects have been added to the edge of the wafer between times that the first and second images thereof are generated.

Claim 19: A wafer edge defect inspection system as defined in claim 17 wherein:

the computer compares and analyzes the first and second images together upon instruction from the user to determine whether any defects have been repaired on the edge of the wafer between times that the first and second images thereof are generated.

Claim 20: A wafer edge defect inspection system as defined in claim 16 incorporated into a fabrication system having a plurality of fabrication stations within which the wafer is subjected to process steps to form integrated circuit components thereon, and wherein:

at least a portion of the located defects are caused by at least one of the process steps to which the wafer is subjected before the image capturing device automatically generates the image of the edge of the wafer.

Evidence Appendix

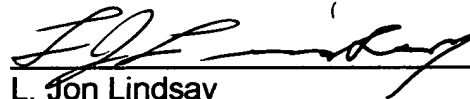
None

Related Proceedings Appendix

None

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Respectfully submitted,



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